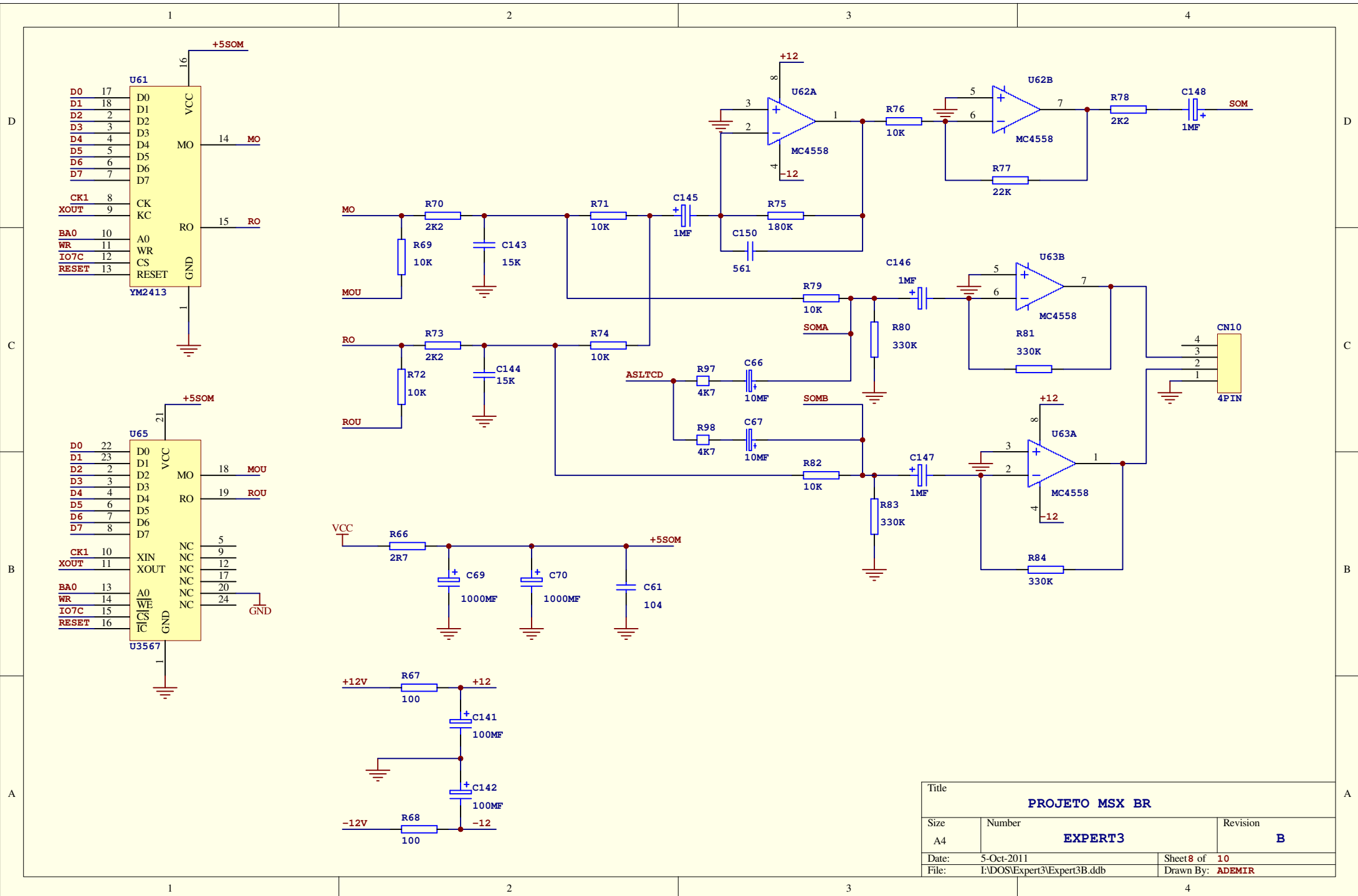
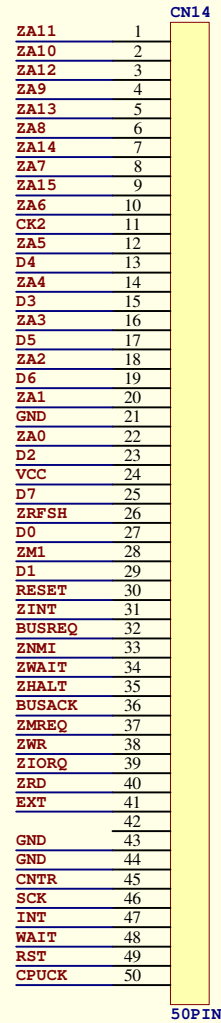
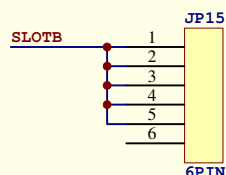
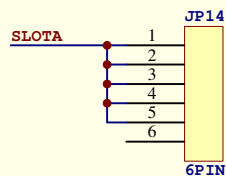
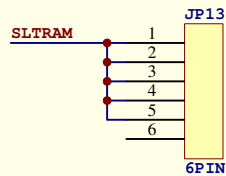
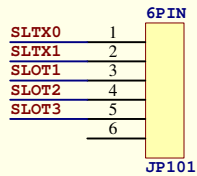
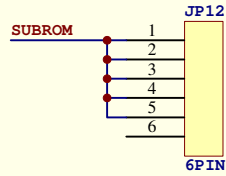
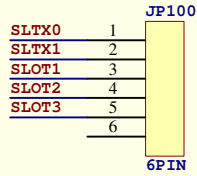
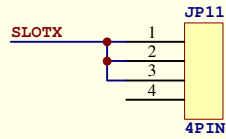
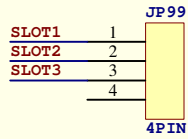


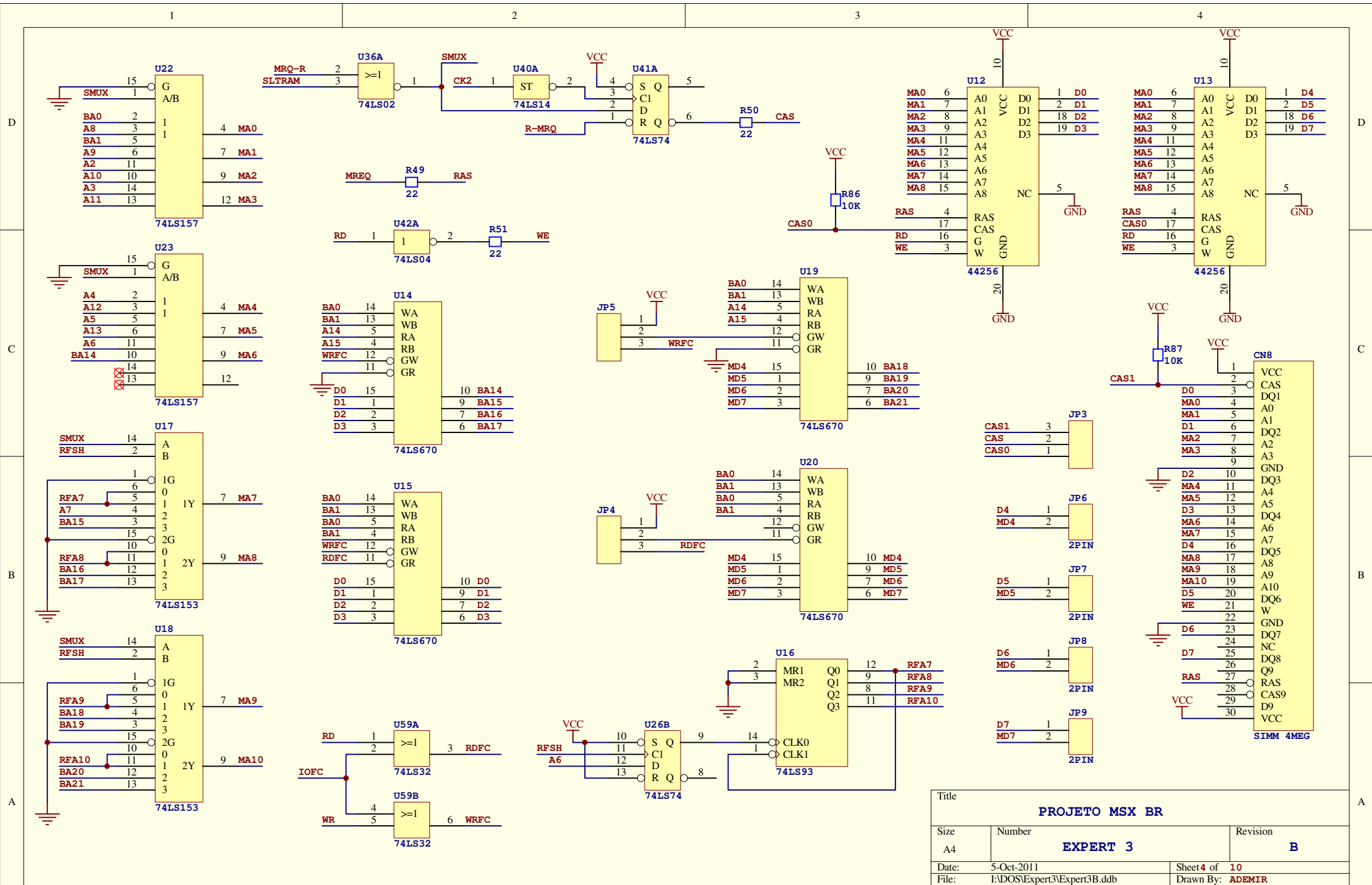
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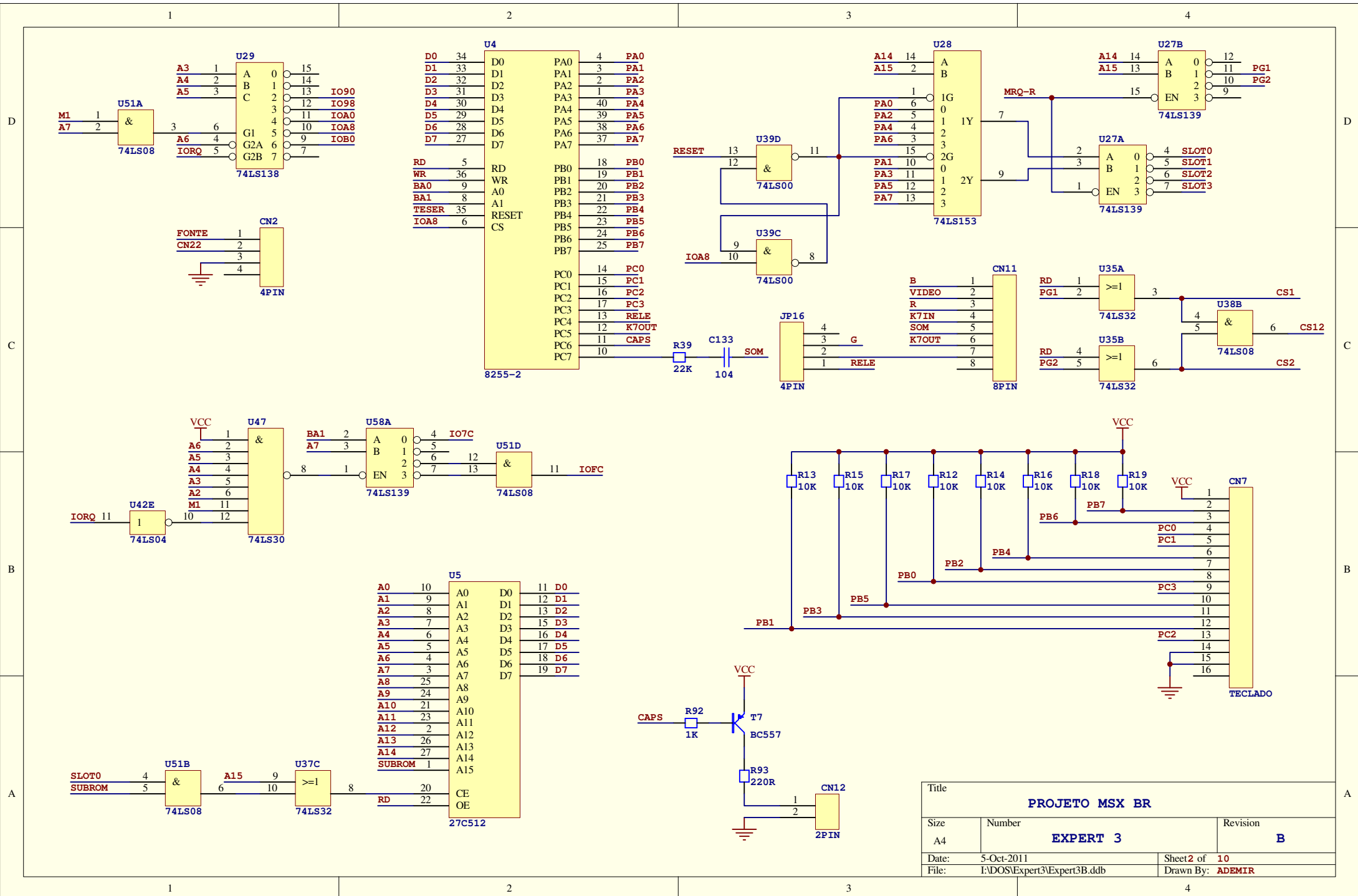


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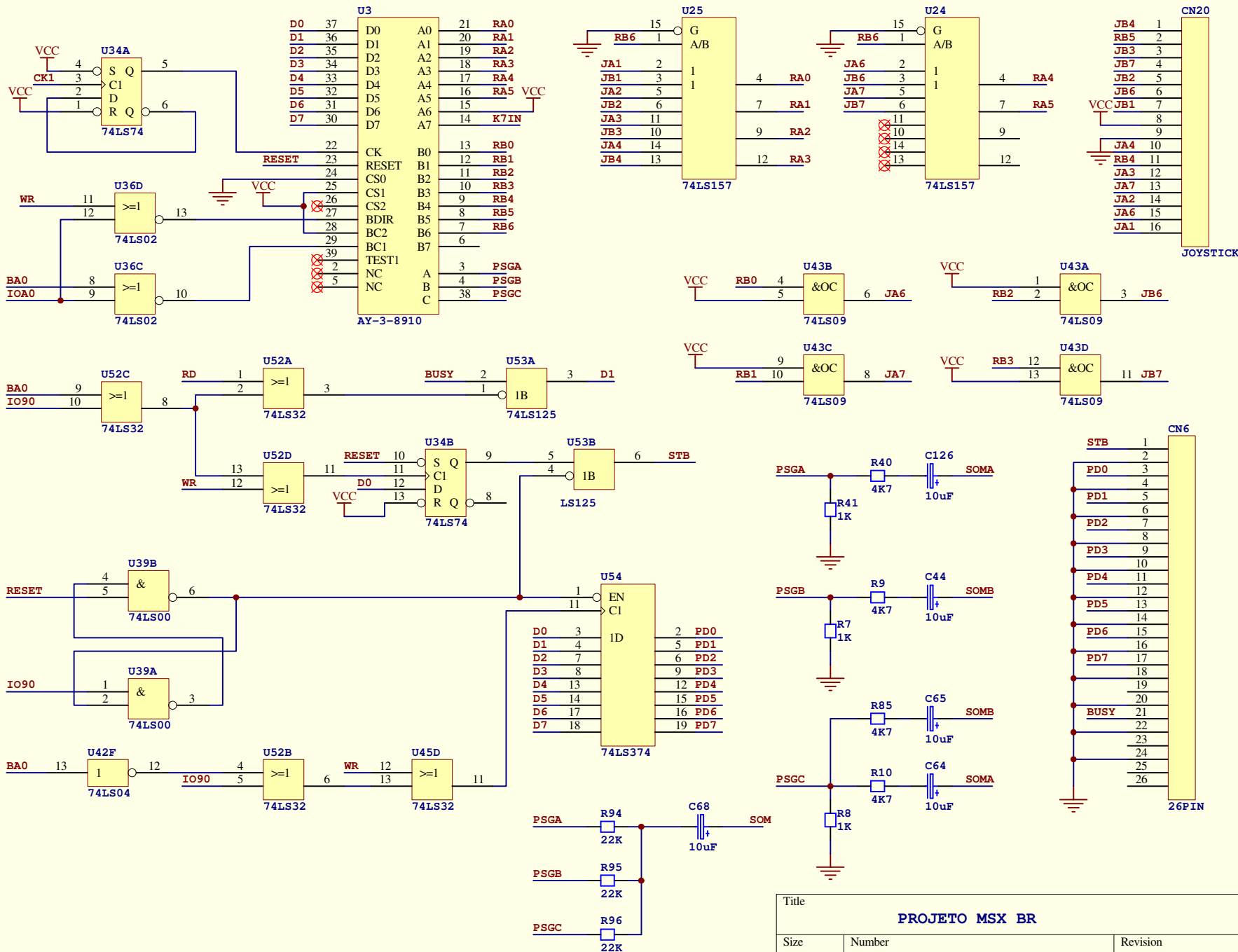


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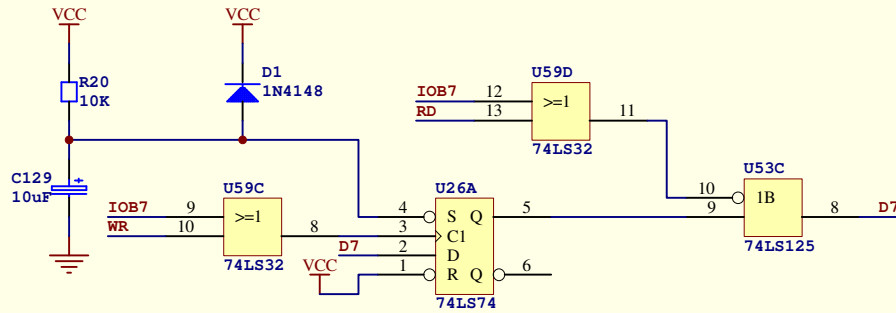
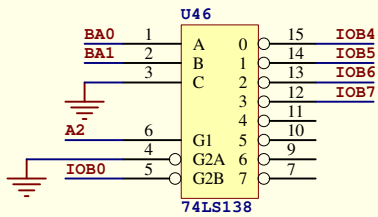
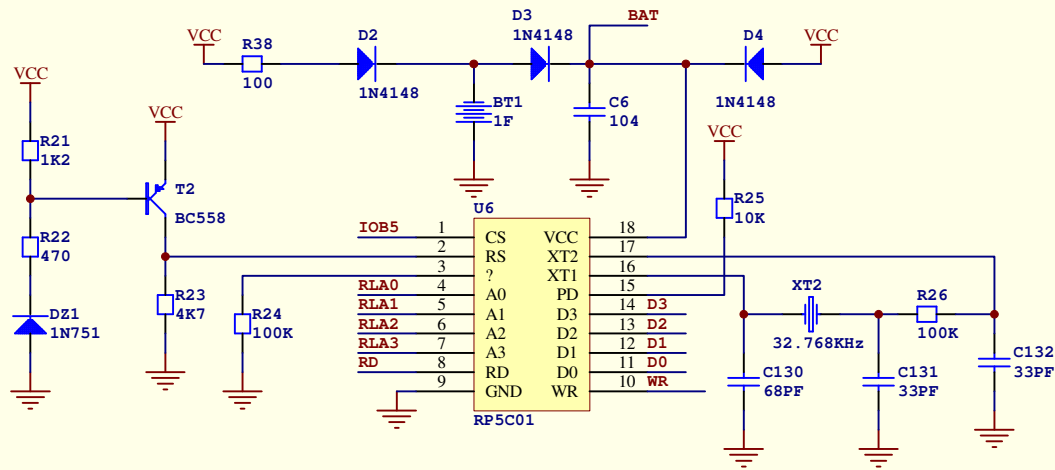
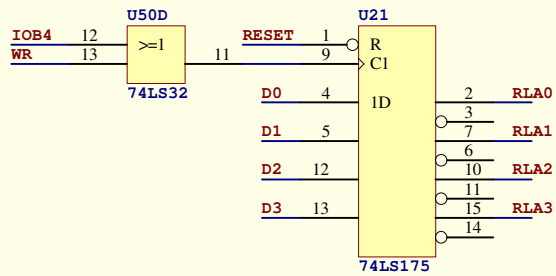
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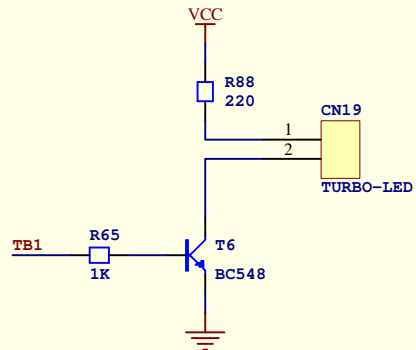
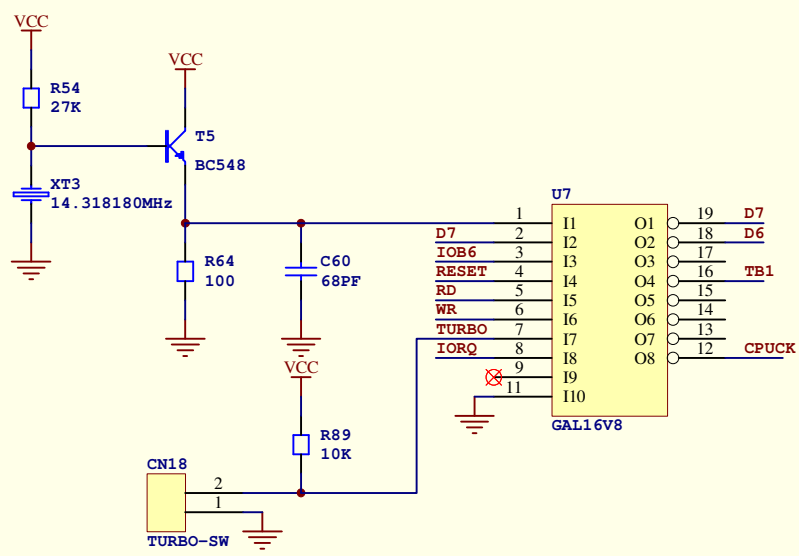
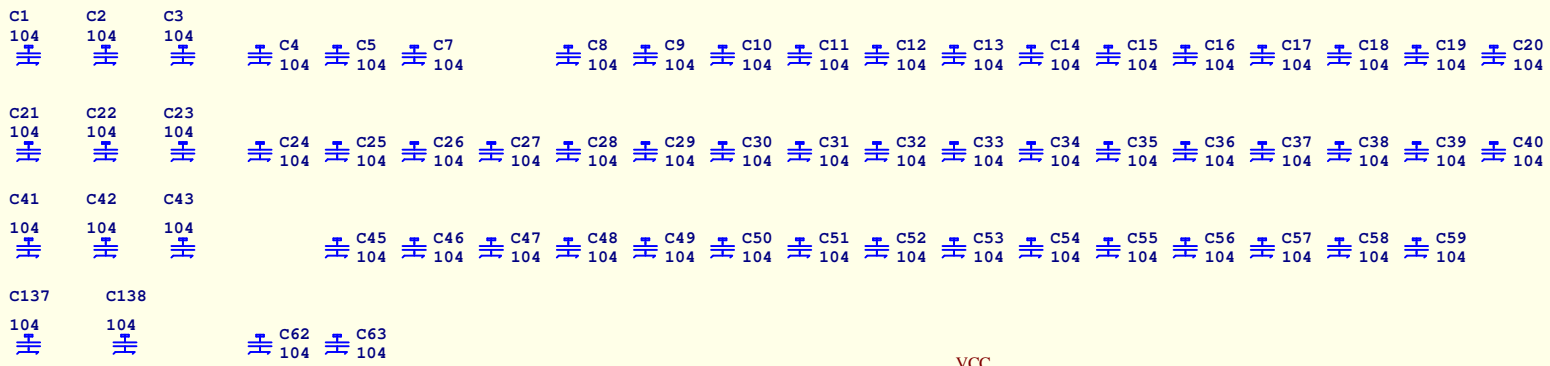
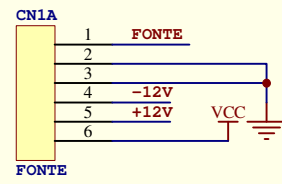
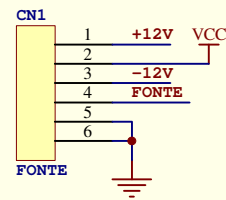
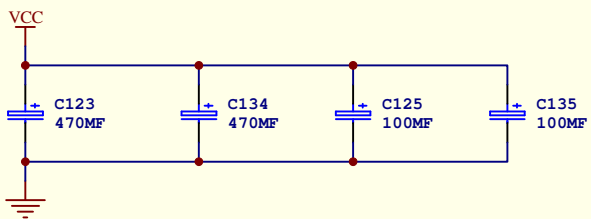
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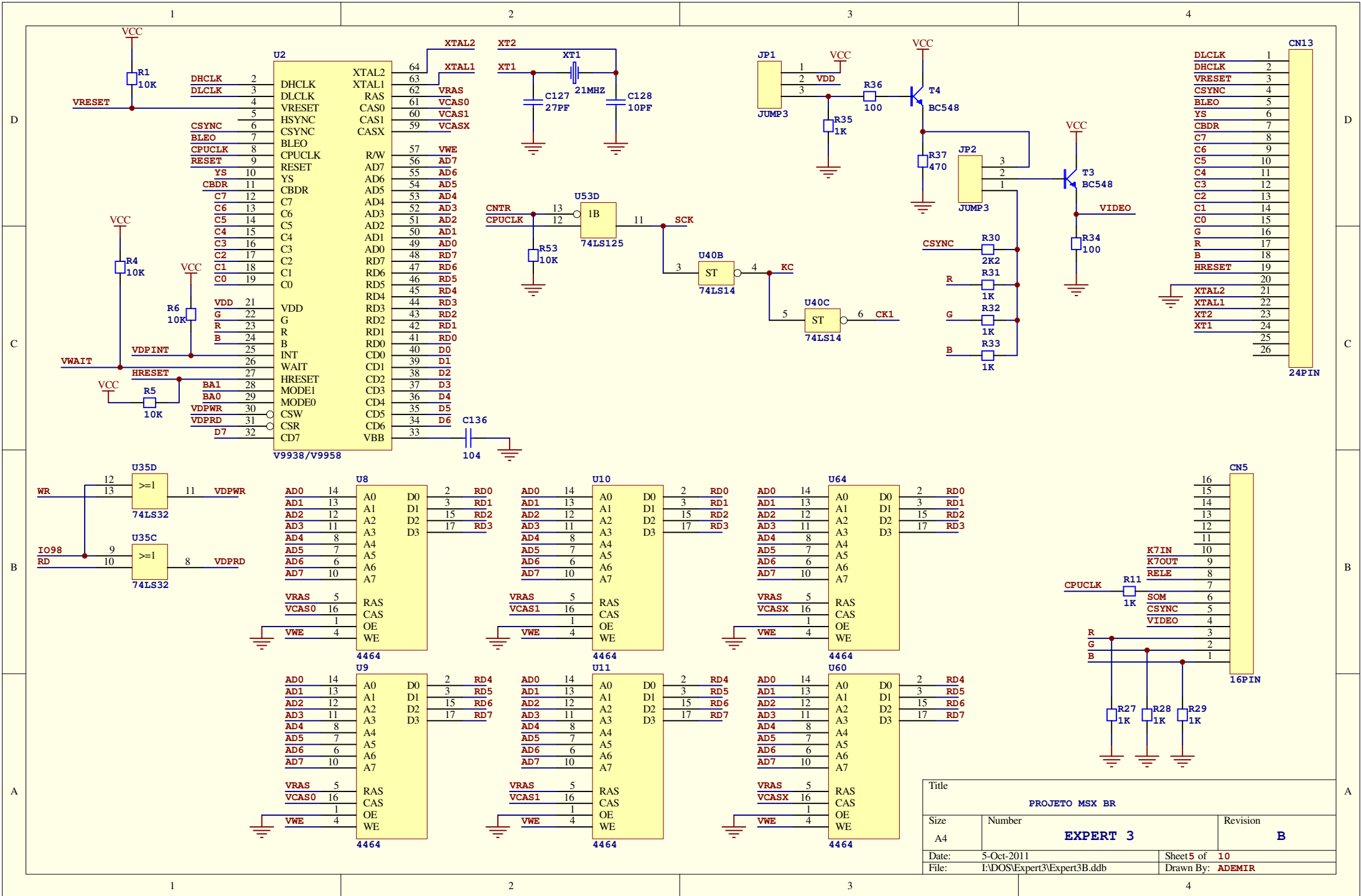
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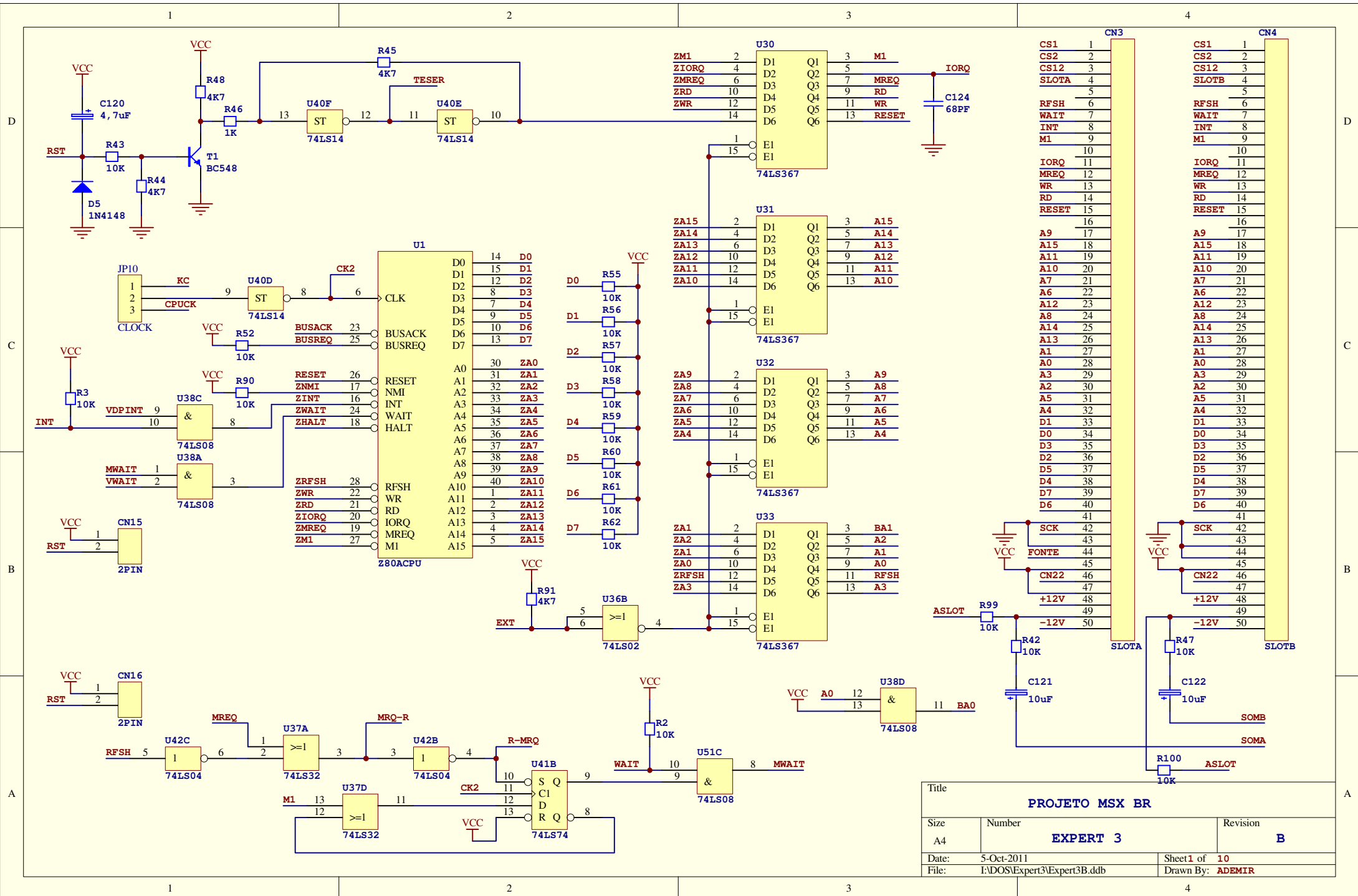
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CS2	2	CS2	2
CS12	3	CS12	3
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RFSH	6	RFSH	6
WAIT	7	WAIT	7
INT	8	INT	8
M1	9	M1	9
	10		10
IORQ	11	IORQ	11
MREQ	12	MREQ	12
WR	13	WR	13
RD	14	RD	14
RESET	15	RESET	15
	16		16
A9	17	A9	17
A15	18	A15	18
A11	19	A11	19
A10	20	A10	20
A7	21	A7	21
A6	22	A6	22
A12	23	A12	23
A8	24	A8	24
A14	25	A14	25
A13	26	A13	26
A1	27	A1	27
A0	28	A0	28
A3	29	A3	29
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D1	33	D1	33
D0	34	D0	34
D3	35	D3	35
D2	36	D2	36
D5	37	D5	37
D4	38	D4	38
D7	39	D7	39
D6	40	D6	40
	41		41
SCK	42	SCK	42
	43		43
FONTE	44	FONTE	44
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-12V	50	-12V	50

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