SVI 738 CLOCK LOGIC – ADD RTC TO SVI WITH EXIST RTC LAYOUT

A lot of schematics exists with different mods how to add the RP5C01 RTC chip, but when I start to investigate how to apply this to get my upgraded SVI (MSX2/2+) machines I very soon discovered that I was not easy to follow and also a lot of the logic was not 100% explain.

I started to test and reverse engineer some of the schematics from Philips, HG version, Original version and Tor's version. (the version that did work and was most documented was Thor's 😊).

I also find a great help from CPC-300 schematics that mostly explain how the RTC works, and how the CS and /CS logic is implemented for the RP5C01 plus the CLK and CLR signal for LS175 chip.

The RICOH datasheet was also good source for try to understand how the RTC works. (all docs are in DOC depot if need for consultation or adaption)

I got really surprised that even if the logic is there is not documented in the SVI Technical Reference Schematic. In my search for knowledge we also document this part in the design.

Part needed for implement the design:

2 x IC sockets (one 18 pins and one 16 pin)

IC 74LS175 and RP5C01

Diode 3 x 1N4118

Capacitors 2 x 30pF, 1 x 22uF 25v, 1 x 0.1uF

Transistor 1 x BC557

1 x Crystal Oscillator 32.768 kHz (2 pins version works fine just ground the top)

Resistors 1 x 4K7, 1 x 1K, 1 x 1K2, 3 x 100K and 1 x 47K

Button Cell socket and a CR2034 battery (no need for recharge, LI-bats work for years 😊)

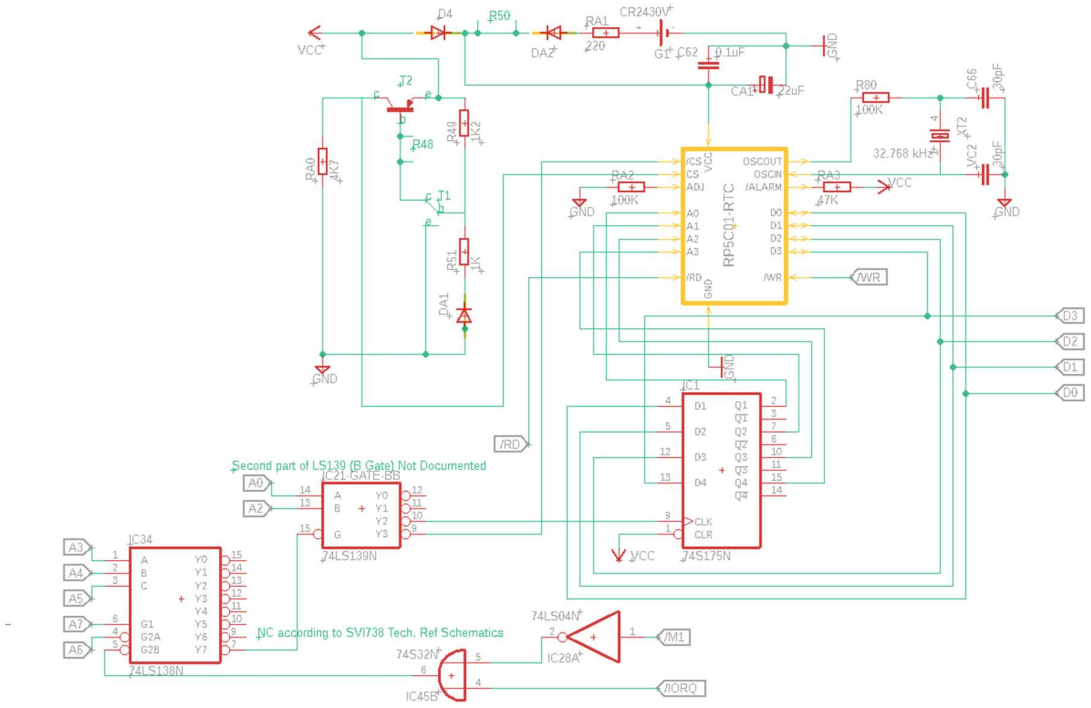
Hook-up wire (AWG30 is recommended) around 5-10cm

Soldering station with regulated heat control, scalpel, flux, de-soldering absorb wire (2 mm) and thin soldering wire, for clean the board after soldering I recommend isopropanol and a new toothbrush.

When de-soldering be careful! Do not overheat and use the de-soldering absorber wire with additional flux to remove the lead from the PCB.

And as always, all MODS & HACKS are done with any responsibility from me or other authors documents or reference!

The Schematic



Let's start by looking at the existing chips on the motherboard that are not documented in the SVI Technical Reference document. IC21 have two gates but only gate A is documented, but by doing some reverse engineering we can see that Y7 is used for the /CS signal to the RTC chip, and Y6 is the CLK signal to the LS175. (this chip is not onboard, but place exists 😊)

The next chips to look at is the LS139 (IC21 Gate B), that is a 2-line to 4-line decoder/demultiplexer and Y4 will enable the /CS port and Y3 will do the CLK to the LS175 chip. This only happens when A0 and A2 is H. (G is L).

INPUTS			OUTPUTS			
ENABLE	SELECT					
/G	B	A	Y0	Y1	Y2	Y4
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Now the G input for the LS139 is handle by IC34 and output line Y7, the LS139 chips is a 1-of-8 Decoder/Demultiplexer. The decoder accepts three binary weighted inputs (A0, A1, A2) and when enabled provides eight mutually exclusive active LOW Outputs (O0–O7). The LS138 features three Enable inputs, two active LOW (E1, E2) and one active HIGH (E3). All outputs will be HIGH unless E1 and E2 are LOW and E3 is HIGH.

TRUTH TABLE													
INPUTS						OUTPUTS							
G1	G2A	G2B	A	B	C	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

The Y7 output on LS138 chip will only be L, when A6-A7 are L plus the combine signal from the OR chipset (LS32 input from /M1 + IORQ) is H and A3-A5 (Inputs A, B and C) are also H. (green marked in table).

Now let's look at the additional IC (LS175) that is added to the board, this the chips are going to be install on position marked on the motherboard as IC19.

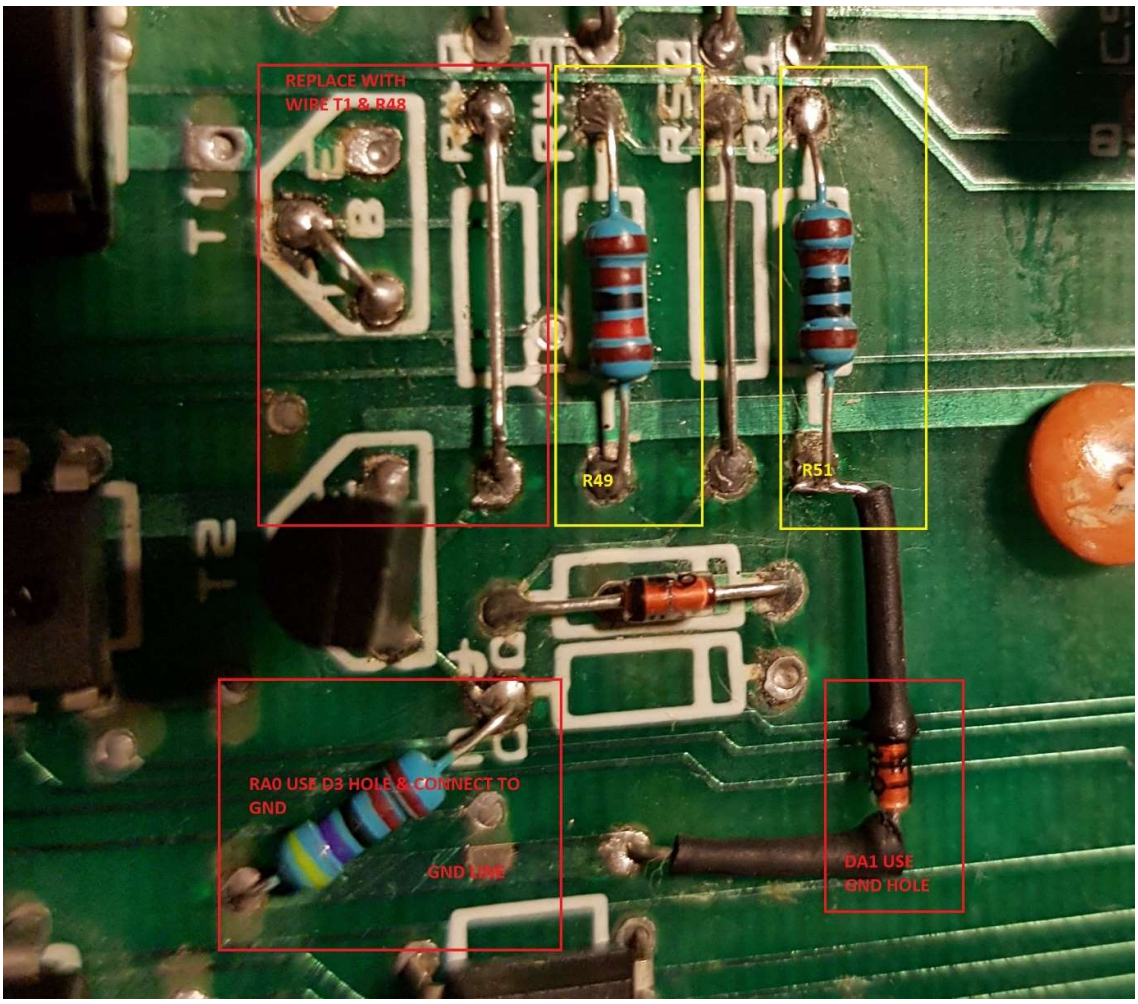
The LS175 is Quad edge-triggered D flip-flops with individual D inputs and Q and Q outputs. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and Q outputs to follow. Master reset is disable because CLR is connected to VCC and always H.

TRUTH TABLE		
Inputs (t=n, MR=H)	Output (t = n+1) Note1	
D	Q	"Q
L	L	H
H	H	L
Note 1: t = n + 1 indicates conditions after next clock.		

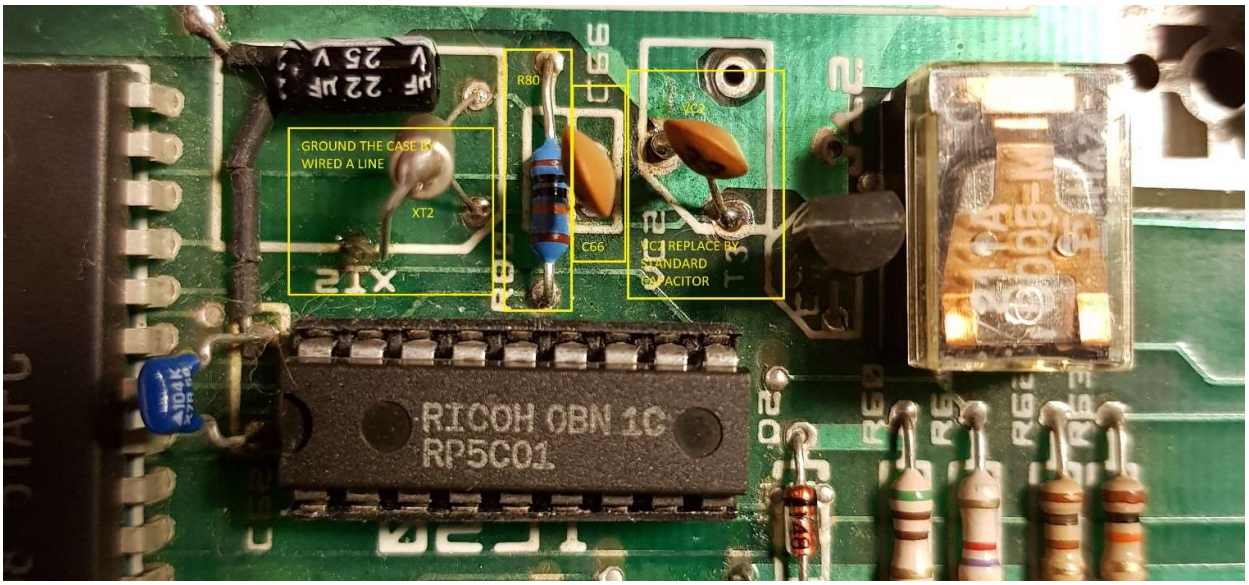
The read and write function to the RTC chip is handle by the /RD and /WR signal also verify by doing reverse engineering.

Last additional chip to install is the RP5C01 and that will be install in IC20 position. The additional CS signal for this chip created by using the RA0, DA1 (additional component not implemented on the motherboard) plus the T2 (BC577), R49 and R51 that are mounted on the board.

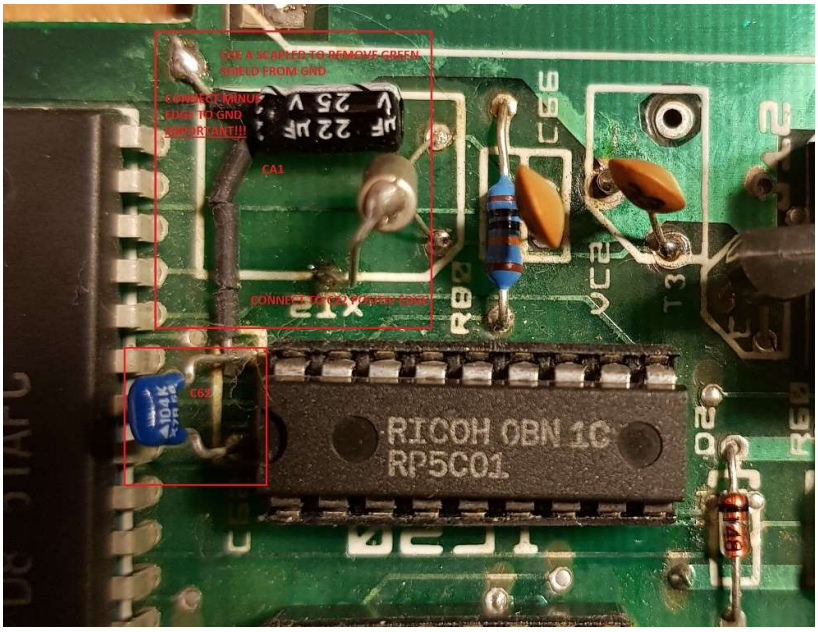
We also replace component R48 and T1 with wired instead. Use the cut part of the R49 and R51 to wire the R48 and T1 (between collector[c] and base [b])



Next part is the oscillator function and those are handled by the R80, XT2, C66 and VC2. The VC2 is here replace by a 30pF capacitor, and XT2 is a 2 pin Crystal Oscillator and you nee to ground the case I recommend use the cut wired from R80 as ground wire.

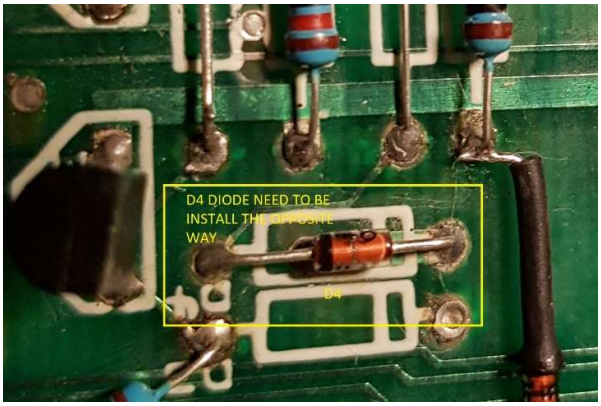


Last part is VCC supply and backup logic for the RTC chip, plus the resistor attached to /ALARM and ADJ. The R50 is replaced by a wired and an additional polarized capacitor is need CA1 (22uF 25V) and positive side is connected to the C62 (0.1uF marked as 104K) and the minus side (marked as -) is connected to ground. (IMPORTANT! will burn if connected wrong)

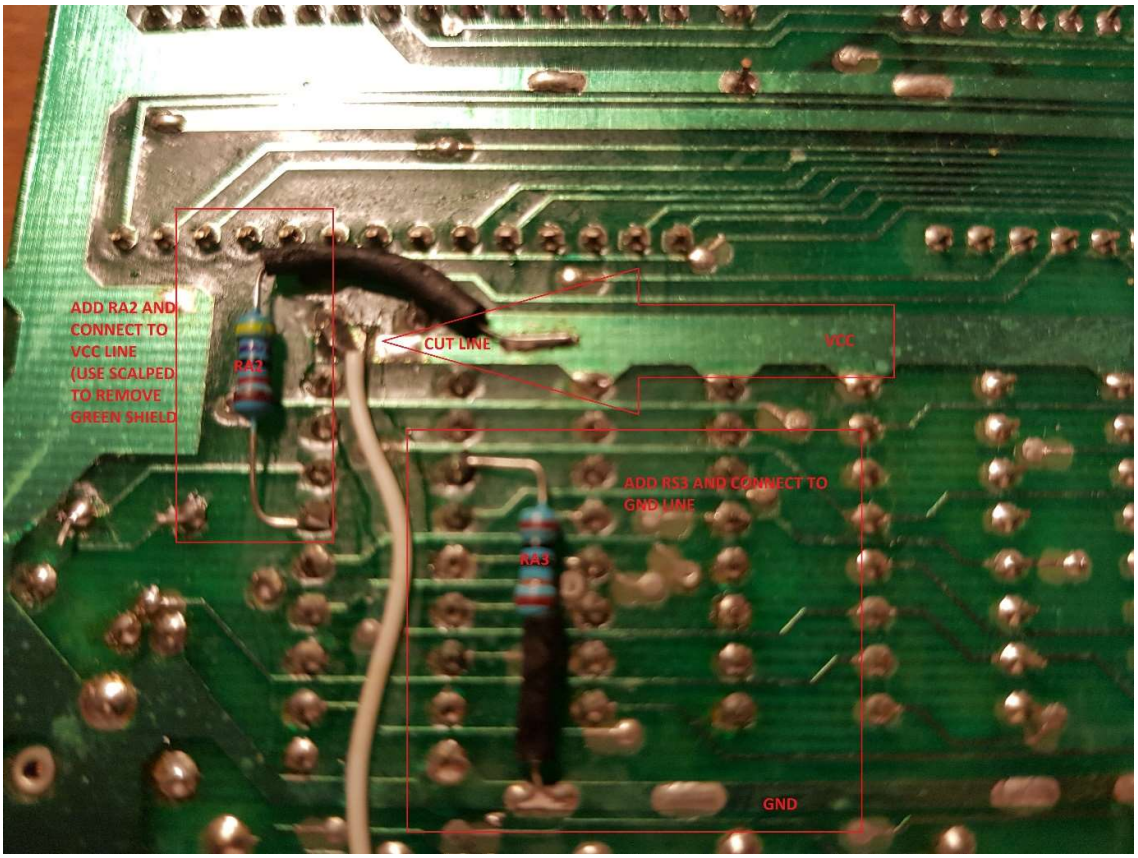


Use the scalped to remove some protected green shield from the ground line. (be carful just the shield not the copper)

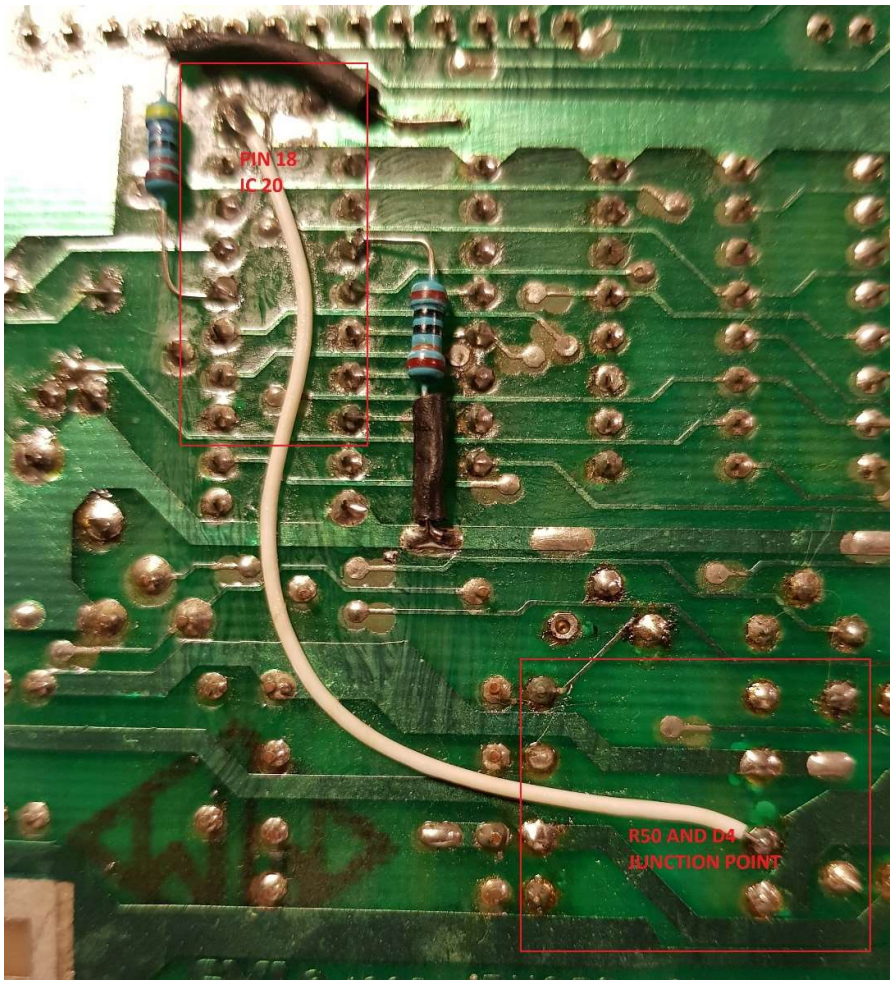
The D4 diode need to be place in the opposite of the schematics on board. (see black ring on diode)



On the backside of the motherboard we need to cut (use the scalped and be careful to not cut any other line) the VCC+ line to PIN 18 on IC20 and add a wire from the junction point where D4 and R50 connect. We also add the additional RA2 and RA3 for ADJ, /ALARM down to GND and VCC.



Use a multi meter to verify that VCC line is cut correctly and to check that junction point is wired correctly to PIN 18 on IC20.



Now the motherboard has the RTC support implemented. 😊

The in theory the schematic can be implemented to add full RTC support to other MSX computers just by adding the discrete components + the RP5C01, LS175, LS138, LS139 and LS04 + LS32 chips.

But a BIOS with RTC support need to available, or the code need to be append to the MSX2/MSX2+ BIOS.